A 21-LEVEL ASYMMETRIC MULTILEVEL INVERTER TOPOLOGY WITH REDUCED SWITCH COUNT

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ABSTRACT :

A 21-level multilevel inverter based on an asymmetric topology is proposed in this work designed optimized for both mid-level and high-power operations requiring high-quality AC output. The design utilizes unequally scaled DC voltage sources along with minimized count of active switching units and diodes to construct layered voltage profiles at the output more efficiently. The system comprises a voltage level generation stage that forms stepped output voltages through selective switching, and a polarity control stage based on a conventional H-bridge to produce bidirectional waveforms. The combined operation results in twenty-one discrete output levels, significantly improving waveform smoothness and reducing total harmonic distortion (THD). This inverter topology also offers benefits such as lower voltage stress across switching devices, reduced switching losses, and minimized filtering needs. Simulation results demonstrate the effectiveness of the configuration in delivering a high-performance AC output suitable for demanding industrial and power electronics systems.

I. INTRODUCTION

With the growing reliance on energy-efficient and renewable technologies, power conversion systems have become integral to modern industrial and utility-scale applications. These systems support various electrical transformations such as, AC to DC, DC to AC, altering DC levels (DC-DC), and transforming AC parameters (AC-AC) and are widely employed in high-voltage transmission, flexible AC systems (FACTS), motor drives, and clean energy platforms like photovoltaic (PV) cells, wind turbines, and fuel cells. Among these, DC to AC conversion is particularly vital, especially when integrating DC sources like solar panels into AC grids. However, conventional inverters, which typically generate three voltage levels ($+V_{dc}$, 0, $-V_{dc}$), produce output waveforms with high harmonic distortion, limiting their suitability for sensitive AC applications.

To address this, multilevel inverters (MLIs) were introduced, offering improved waveform quality through a stepped voltage output that closely approximates a sine wave. MLIs also reduce Overall harmonic content (THD), voltage stress on switches, and filtering requirements, making them ideal for use in medium and large-scale power systems. Various MLI topologies as exemplified by diode-clamped, flying capacitor, and cascaded H-bridge have been analysed, each offering distinct

advantages in terms of efficiency and complexity. Furthermore, MLIs can be designed using either symmetrical (equal DC voltages) or asymmetrical (unequal DC voltages) configurations, with the latter enabling more output levels with fewer components. Despite these benefits, MLIs still pose challenges related to control complexity and increased component count, which continue to drive research in topology optimization and modulation strategies.

II. ASYMMETRIC 21-LEVEL INVERTER CIRCUIT DESIGN

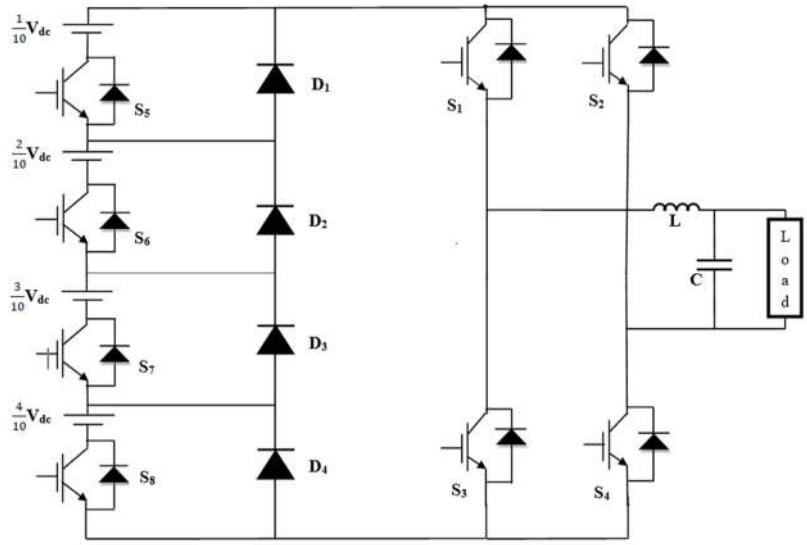

Fig.1. Asymmetric 21-Level Inverter Circuit Design.

The circuit diagram in Fig. 1 shows a 21-level asymmetric cascaded multilevel inverter (MLI) configuration designed to produce a high-quality stepped AC output using a reduced number of components. This topology consists of two main functional sections: voltage level generation and polarity generation.

1. Voltage Level Generation Unit

Located on the left side of the circuit, this stage is responsible for constructing discrete voltage steps using four asymmetrical DC voltage sources rated as:

$$\frac{1}{10}V_{dc}, \frac{2}{10}V_{dc}, \frac{3}{10}V_{dc}, \frac{4}{10}V_{dc}$$

These sources are connected in series via four controlled switches (S_5 to S_8) and four diodes (D_1 to D_4). By selectively turning ON/OFF the switches, different combinations of the DC voltages assumed to generate output voltages ranging from $\frac{1}{10}V_{dc}$ up to V_{dc} in ten steps. Diodes D_1–D_4 ensure unidirectional conduction and prevent reverse current flow between the voltage sources. The design

follows an asymmetric configuration, meaning the DC sources are of different magnitudes, which allows more voltage levels with fewer sources and switches.

2. Polarity Generation Unit

The right-hand part of the circuit comprises a conventional H-bridge made up of four switches (S_1 to S_4) and associated anti-parallel diodes. This full-bridge setup handles the polarity reversal of the voltage generated from the left section. By switching specific pairs (e.g., S_1 & S_4 or S_2 & S_3), the same voltage magnitude can be applied with either positive or negative polarity across the load.

3. Output Voltage Profile

This inverter produces:

- 10 positive levels (from $\frac{1}{10}V_{dc}$ to V_{dc}),
- 10 negative levels (from $-\frac{1}{10}V_{dc}$ to $-V_{dc}$),
- and a zero level when the output is shorted or bypassed.

Thus, it synthesizes a total of **21 discrete voltage levels**, offering a high-resolution approximation of a sinusoidal waveform with significantly reduced harmonic content.

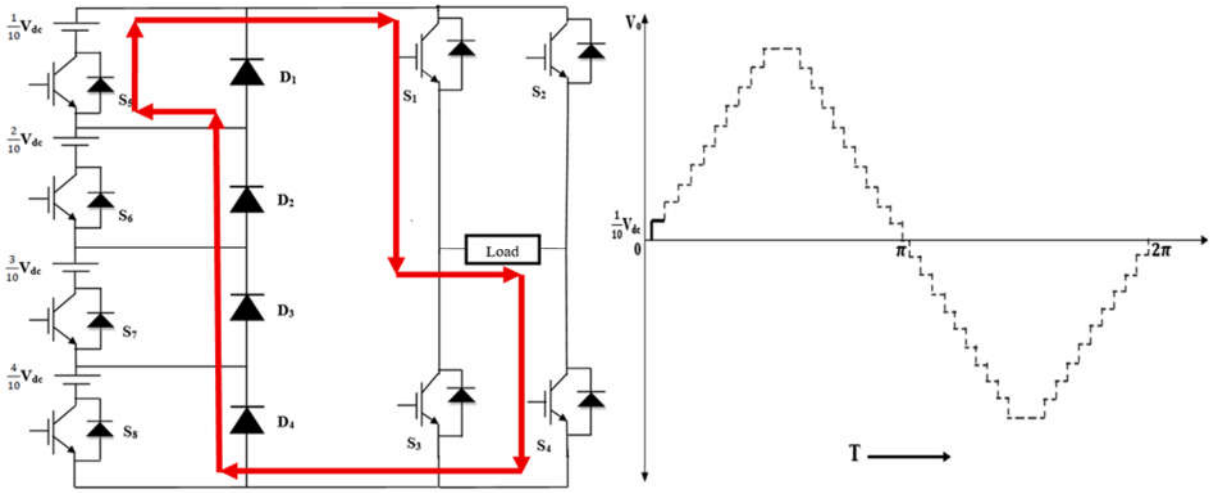

Fig. 2 (a) Generation of $\frac{1}{10}V_{dc}$ Output Level in a 21-Level Inverter Using Selective Switching.

In a 21-level inverter, the output level of $\frac{1}{10}V_{dc}$ is generated by activating switch S_5 and the polarity control switches S_1 and S_4. Switch S5 links the smallest DC voltage source to the circuit, while S_1 and S_4 guide the current flow through the load in the intended direction. This setup results in the lowest positive voltage step in the output waveform.

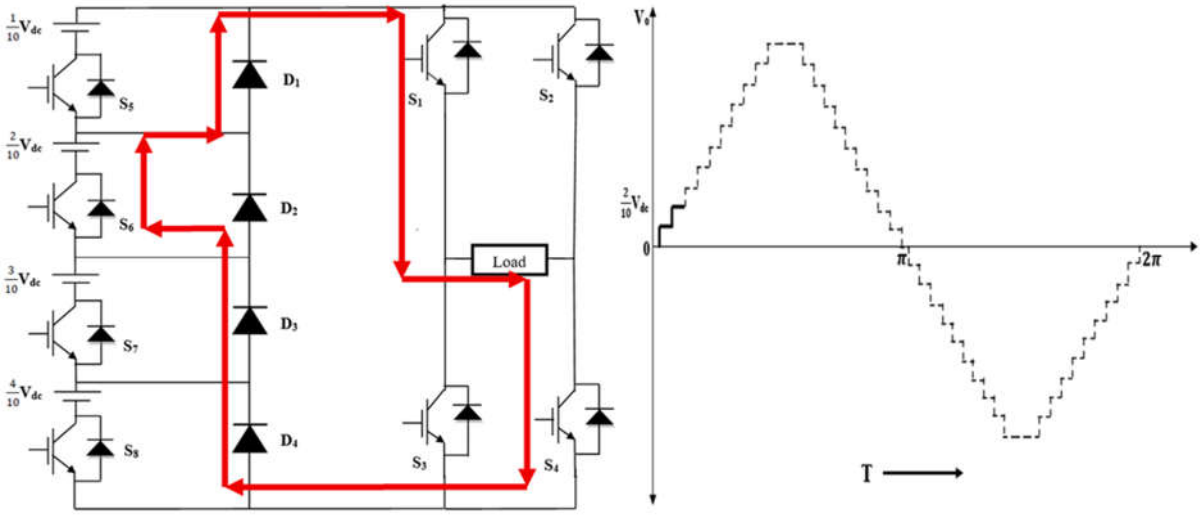

Fig. 2 (b) Generation of Output Level $\frac{2}{10}V_{dc}$ in a 21-Level Inverter Through Controlled Switching.

The $\frac{2}{10}V_{dc}$ output level is achieved by turning on switch S6 along with polarity switches S_1 and S_4. Switch S_6 connects the second DC source in the stack, while S_1 and S_4 direct the current through the load with the correct polarity. This switching combination produces the second positive voltage step in the multilevel output waveform.

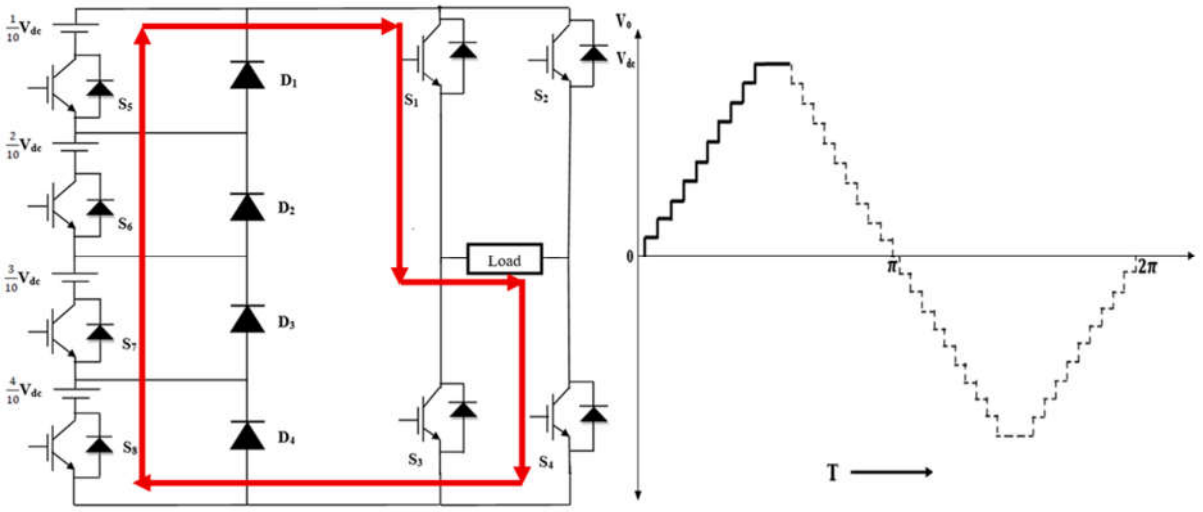

Fig. 2 (c) Generation of Maximum Output Voltage V_{dc} in a 21-Level Inverter Using Full DC Source Activation.

The full output voltage V_{dc} is produced by turning on switches S_5, S_6, S_7, and S_8 along with polarity switches S_1 and S_4. This combination connects all four DC sources in series, delivering the total DC voltage across the load. The polarity switches direct the current flow, generating the highest positive step in the output waveform.

This inverter topology is designed to generate 21 output voltage levels using only 8 power switches. The switching table provides binary states (1 = ON, 0 = OFF) for each switch to achieve specific output voltages ranging from $-V_{dc}$ to $+V_{dc}$ in fine steps of $\frac{1}{10}V_{dc}$.

Voltage Levels	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
(1/10) V_{dc}	1	0	0	1	1	0	0	0
(2/10) V_{dc}	1	0	0	1	0	1	0	0
(3/10) V_{dc}	1	0	0	1	0	0	1	0
(4/10) V_{dc}	1	0	0	1	0	0	0	1
(5/10) V_{dc}	1	0	0	1	1	0	0	1
(6/10) V_{dc}	1	0	0	1	0	1	0	1
(7/10) V_{dc}	1	0	0	1	0	0	1	1
(8/10) V_{dc}	1	0	0	1	1	0	0	1
(9/10) V_{dc}	1	0	0	1	0	1	1	1
V_{dc}	1	0	0	1	1	1	1	1
(0V) V_{dc}	0	0	1	1	0	0	0	0
-(1/10) V_{dc}	0	1	1	0	1	0	0	0
-(2/10) V_{dc}	0	1	1	0	0	1	0	0
-(3/10) V_{dc}	0	1	1	0	0	0	1	0
-(4/10) V_{dc}	0	1	1	0	0	0	0	1
-(5/10) V_{dc}	0	1	1	0	1	0	0	1
-(6/10) V_{dc}	0	1	1	0	0	1	0	1
-(7/10) V_{dc}	0	1	1	0	0	0	1	1
-(8/10) V_{dc}	0	1	1	0	1	0	0	1
-(9/10) V_{dc}	0	1	1	0	0	1	1	1
- V_{dc}	0	1	1	0	1	1	1	1

Table 1. Switching Pattern for 8 Switching Devices.

- **Advantages of the Configuration**

1. Fewer switches required for high-level output.
2. Accurate voltage level synthesis ensures lower THD in the output signal.
3. In contrast to traditional two-level topologies, the switch voltage handling requirement is substantially reduced.
4. Improved efficiency with optimized switching operation and minimal filtering needs.

- **Applicability**

The inverter is well-adapted for industrial systems operating at medium and high voltage levels, motor drives, or UPS systems where precise AC output is essential, and high-power quality is required.

III. MODULATION STRATEGY FOR 21-LEVEL INVERTER

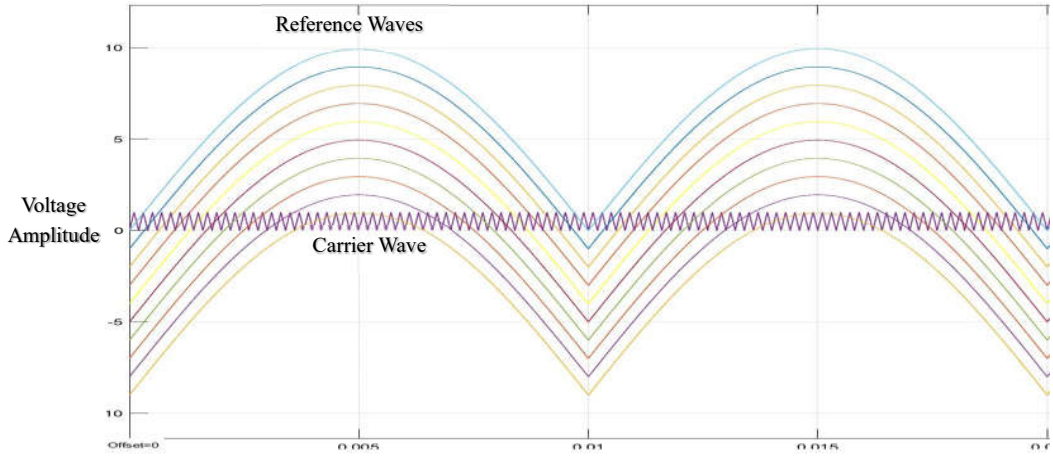

Fig. 4. Comparison-Based Modulation Using Carrier Wave and Ten Sinusoidal References.

To achieve a 21-level discrete output voltage in the developed inverter configuration, a modulation technique Phase Disposition PWM (PD-PWM) modulation strategy is adopted that utilizes ten identical sine wave references, each having an amplitude of 9.95, alongside a single triangular carrier waveform operating at 5 kHz. These reference signals are synchronized in phase and frequency and are spaced to represent incremental voltage divisions between $-V_{dc}$ and $+V_{dc}$. Each of these sine waves is compared simultaneously against the high-frequency triangular waveform using comparator circuits, producing a set of digital signals that indicate which voltage segment should be active at a given time. These signals are passed through a structured logic network comprising basic logic gates such as AND, OR, and NOT to generate appropriate gate pulses for the inverter's eight switches (S_1 to S_8). The switches S_5 through S_8 are responsible for selecting the voltage magnitude from fractional DC voltage sources, while switches S_1 to S_4 form an H-bridge arrangement that determines the polarity of the output waveform. This approach enables supporting the inverter in achieving a well-defined multistep waveform, effectively approximating a waveform similar to a sine function and mitigating harmonic interference. Moreover, using a single high-speed carrier simplifies the control logic while ensuring accurate and efficient switching, making the method practical for medium-power applications requiring high-quality AC output.

The modulation amplitude (M_a) is defined as the ratio of the reference signal amplitude to the total effective amplitude of the carrier signals used in the comparison process. The expression for M_a is given by:

$$M_a = \frac{Am}{(n*Ac)}$$

Where:

- A_m is the peak value of each sine reference signal,
- A_c is the peak value of the triangular carrier signal,
- n is the number of levels per polarity, which can be calculated as:

$$n = \frac{L-1}{2}$$

where L denotes the total number of voltage levels produced by the inverter.

For this design:

- A_m=9.95 V,
- A_c=1V,
- L=21, hence n=10

Substituting these values:

$$M_a = \frac{9.95}{(10*1)}$$

$$M_a = 0.995$$

This value of modulation amplitude confirms that the inverter operates within the linear modulation range, ensuring efficient utilization of the input DC voltage and maintaining high output waveform fidelity.

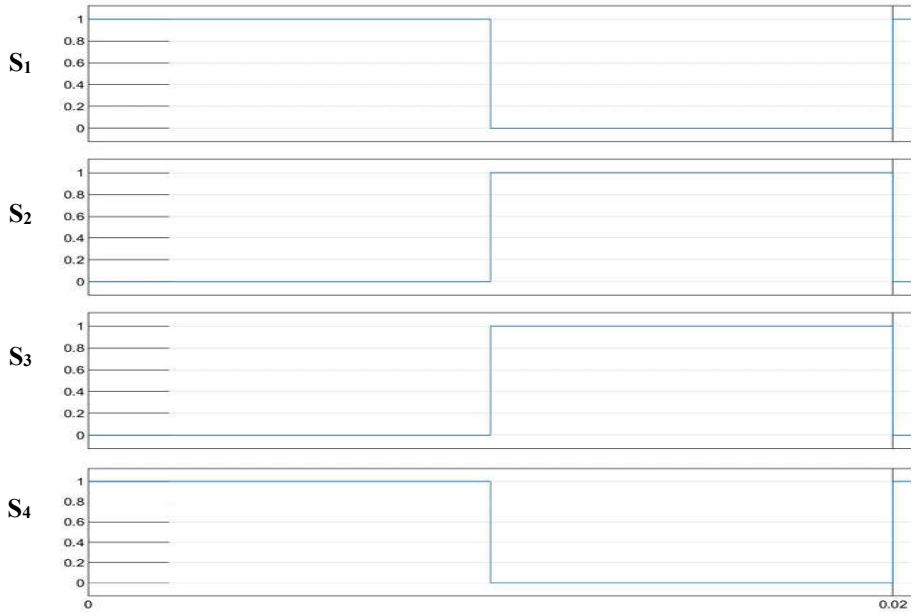

Fig. 5. Gating Signals Corresponding to S_1, S_2, S_3 and S_4.

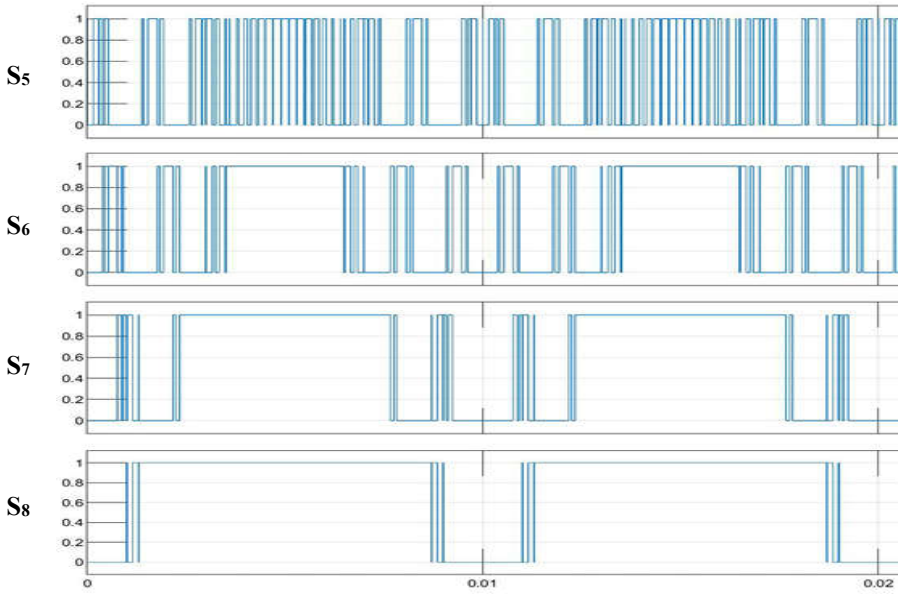

Fig. 6. Gate Drive Signals for S_5, S_6, S_7 and S_8.

IV. SIMULATION RESULTS

A 21-level asymmetric multilevel inverter is modelled in Simulink using 4 unequal DC sources, 8 IGBT switches, and 4 current-directing diodes with R-load of 26.45Ω. Gate pulses are generated using a PWM strategy to produce a finely stepped output waveform. The design achieves a low THD (~1.3%), confirming its effectiveness in delivering a near-sinusoidal output across an R-load. The reduced component count and simple control make it suitable for renewable and medium-power applications.

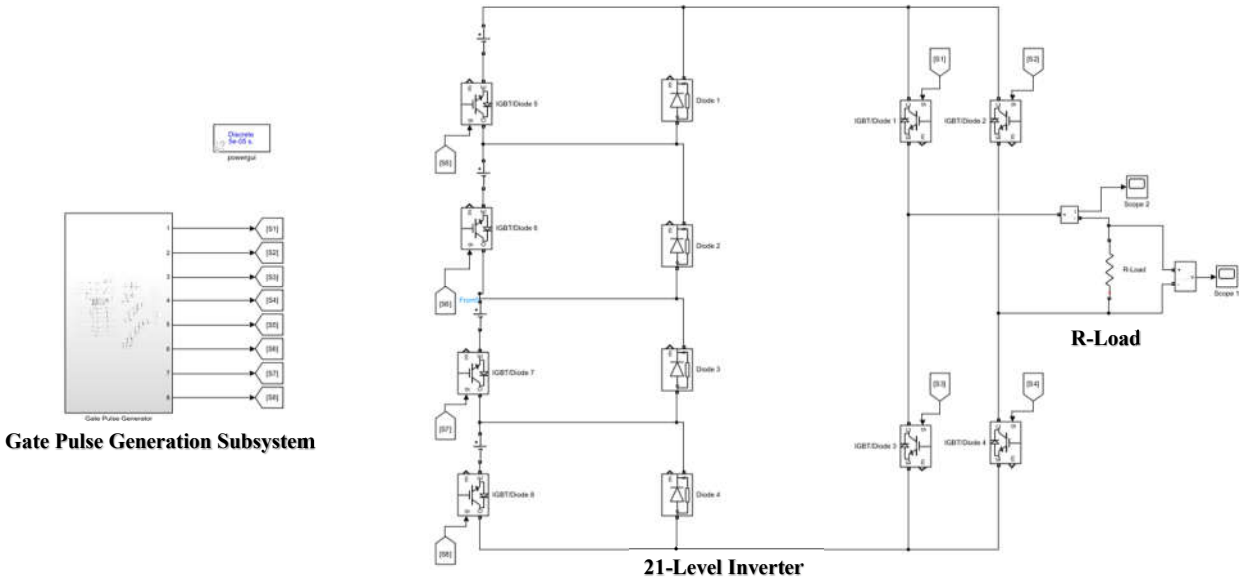

Fig. 7. MATLAB/Simulink Design of the 21-Level Asymmetric Topology

A. Output Voltage Current Waveform and Harmonic Distortion Analysis

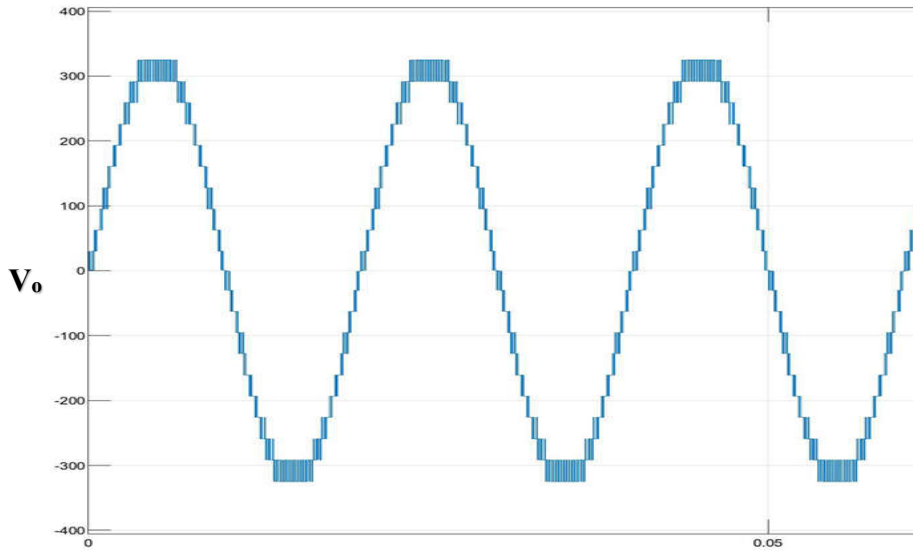

Fig. 8. Stepped Voltage Waveform with 21 Levels.

Figure 8 displays the final output voltage pattern of the implemented 21-level inverter. The waveform exhibits a near-sinusoidal shape composed of multiple discrete steps, characteristic of multilevel inverter topologies. These stepped levels help to reduce the voltage stress across switching devices and enhance the overall waveform quality. The output voltage reaches a peak of approximately ±326 V, indicating that the inverter effectively produces the desired fundamental voltage magnitude.

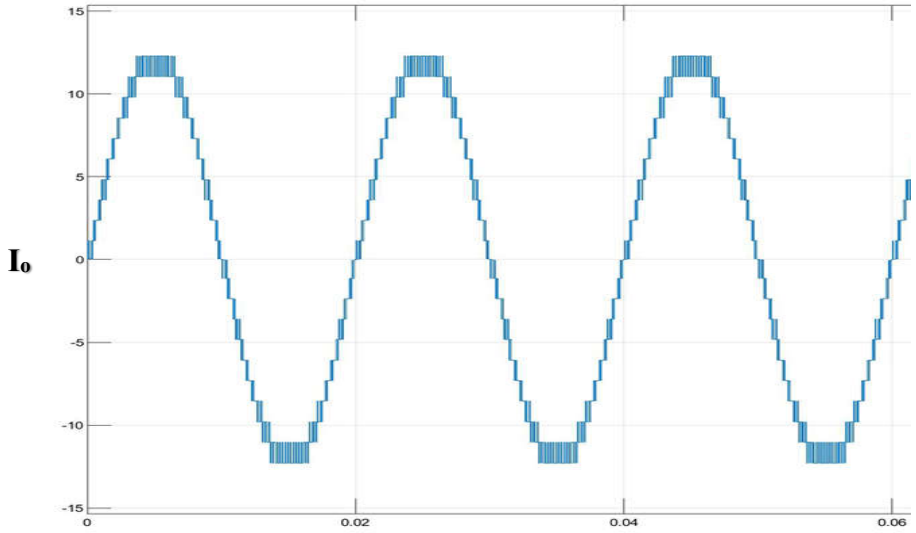

Fig. 9. Measured Load Current at the Inverter Output.

Figure 9 shows the load current corresponding to the stepped voltage waveform. The current is smooth and nearly sinusoidal, demonstrating efficient operation and proper filtering. The peak current amplitude is about ±13 A, confirming that the inverter delivers a stable and low-distortion current to the load.

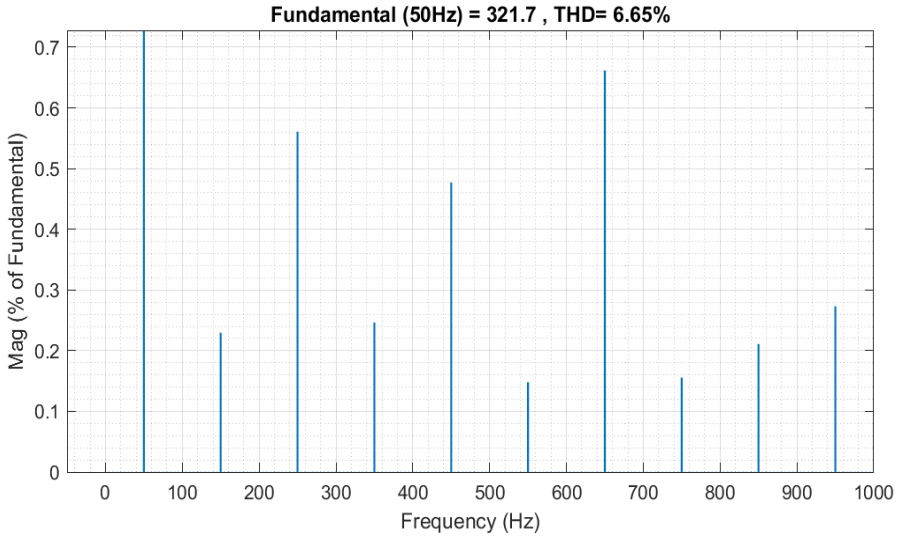

Fig. 10. THD Measurement for the Output of the 21-Level Inverter.

Fourier spectrum of the inverter output, shown in chart 10, provides insight into the harmonic performance. The base frequency observed at has a with an amplitude measuring 321.7 V. The harmonic analysis yields a THD of 6.65%, which reflects a significant reduction in harmonics in contrast with conventional two-level inverter systems. This relatively low THD is attributed to the multilevel structure and the appropriate pulse width modulation (PWM) strategy employed.

B. Improved Output Voltage and Current Quality Using LC Filter: Waveform and THD Analysis

➢ Design of LC Low-Pass Filter for an RL Load

To suppress high-frequency switching harmonics from a PWM inverter while maintaining a smooth sinusoidal output at 50 Hz, an LC low-pass filter is implemented. The filter is designed to operate with an R load rated at 2 kW, with a resistance of 26.45 Ω.

1. Selection of Cutoff Frequency

The cutoff frequency of the filter must be higher than the fundamental frequency (50 Hz) but significantly lower than the inverter switching frequency to effectively attenuate harmonics. Considering a switching frequency f_{sw}=5 kHz, a suitable cutoff frequency is selected as:

$$f_c = 20\%\ f_{sw}$$

$$f_c = 0.2 * 5000$$

$$f_c = 1000\text{Hz}$$

2. LC Product Calculation

The cutoff frequency of an LC low-pass filter is related to the inductance L and capacitance C by the expression:

$$f_c = \frac{1}{2\pi\sqrt{LC}}$$

$$LC = \frac{1}{(2\pi fc)^2}$$

$$LC = \frac{1}{(2\pi * 1000)^2}$$

$$LC = 2.533 * 10^{-8} HF$$

3. Component Selection

Assuming an inductance of L=3mH, which is practical and commonly available for power filter applications, the corresponding capacitance is calculated as:

$$C = \frac{LC}{L}$$

$$C = \frac{2.533 * 10^{-8}}{3 * 10^{-3}}$$

$$C = 8.44\ \mu F$$

- **Final Filter Parameters**

- Inductance (L): 3 mH
- Capacitance (C): 8.44 µF
- Cutoff Frequency: ≈ 1 kHz
- Load Resistance: 26.45 Ω

This LC filter ensures effective attenuation of switching harmonics while allowing the 50 Hz fundamental component to pass with minimal distortion, making it suitable for grid-connected inverter applications.

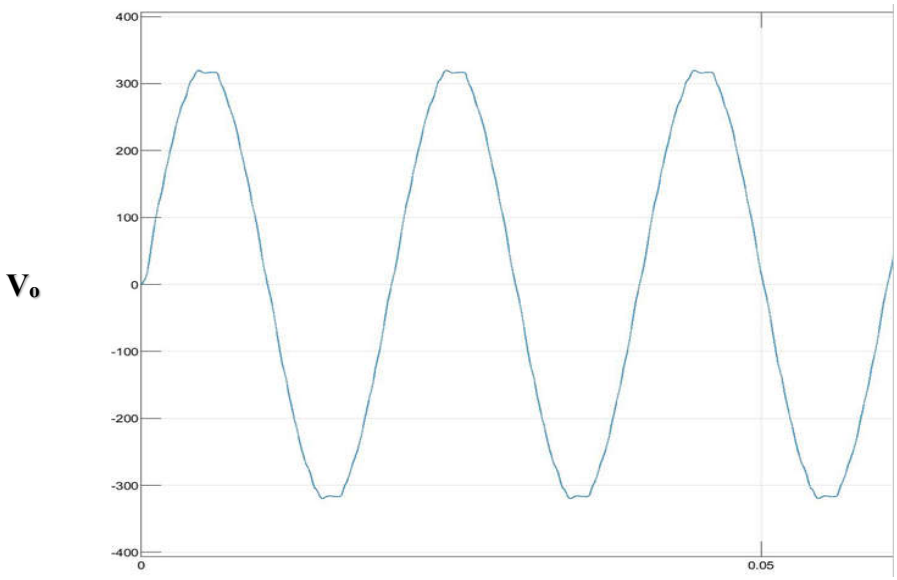

Fig. 11. Output Voltage Profile with Low-Pass LC Filter.

The implementation of a 3 mH inductor and an 8.5 µF capacitor as an LC filter significantly enhances the purity of the voltage signal produced by the inverter. As shown in Figure 1, the output voltage waveform becomes highly sinusoidal with a smooth profile and negligible visible distortions. The peak voltage remains around ±322 V, closely maintaining the desired amplitude for the fundamental frequency.

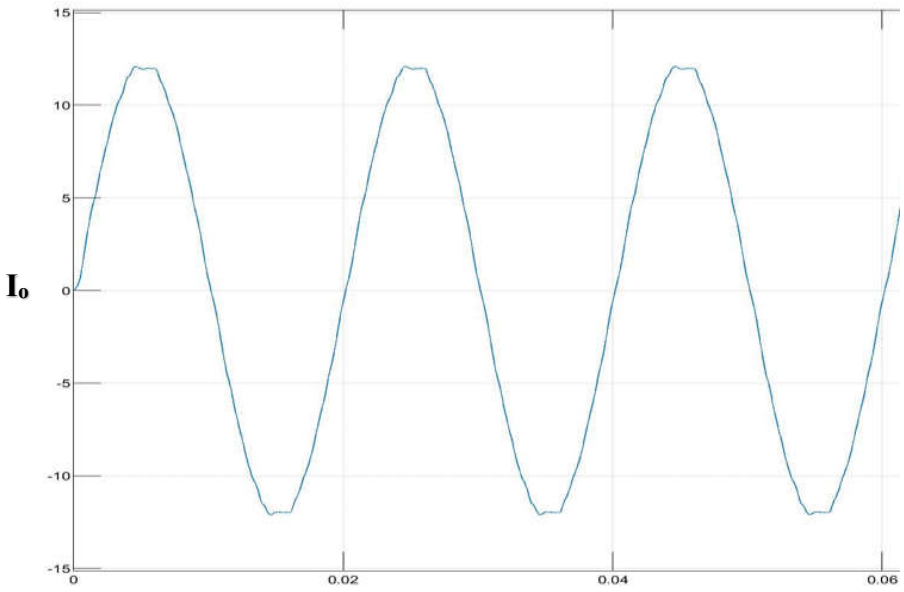

Fig. 12. LC Filtered Load Current Response.

Similarly, the load current shown in Figure 12 is also highly sinusoidal with minimal ripple, indicating effective filtering and proper power delivery to the load. The current reaches peak values of approximately ±13 A, reflecting stable operation.

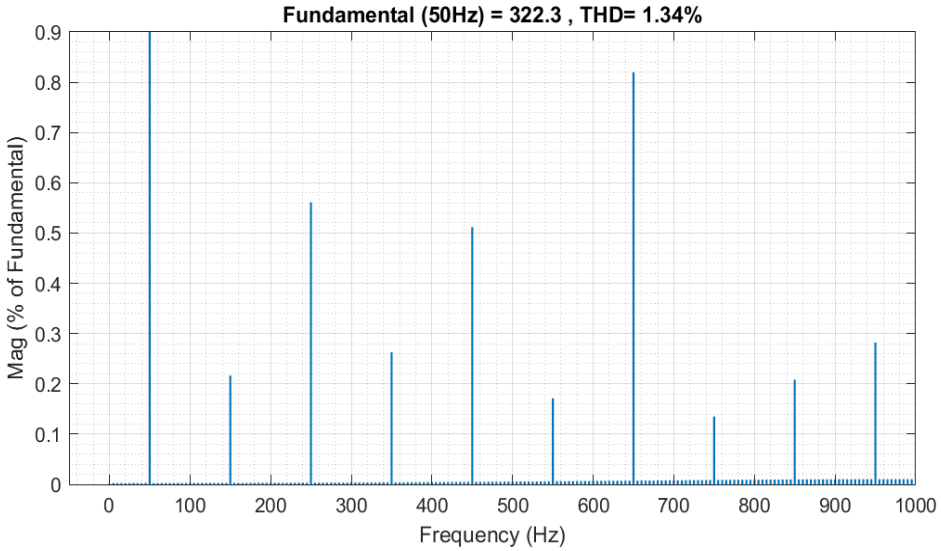

Fig. 13. THD Measurement for the Output of the 21-Level Inverter with LC filter.

The frequency spectrum in Figure 13 reveals a base frequency component at 50 Hz with an amplitude of 322.3 V. A low THD value of 1.34% is obtained, highlighting the effectiveness of the LC filter in suppressing high-frequency harmonics. Compared to the unfiltered case, this represents a significant improvement in waveform purity, making the output more suitable for sensitive loads and grid-tied applications.

V. COMPARATIVE EVALUATION OF 21-LEVEL MULTILEVEL INVERTER TOPOLOGIES

Criteria	Proposed Asymmetric 21-Level Inverter	Symmetric 21-Level Inverter	Diode-Clamped (NPC)	Flying Capacitor (FC)	Cascaded H-Bridge (CHB)
DC Sources	4 (with unequal voltage levels)	10 equal sources	1	1	10 (1 per H-bridge)
Switches (IGBTs/MOSFETs)	8	20	40	40	40 (4 per H-bridge × 10)
Diodes	4 (for unidirectional current flow)	0	~180 (clamping diodes)	0	0
Capacitors	0	0	0	~180	0
Control Complexity	Moderate	Simple	High	Very High	Moderate
Total Harmonic Distortion (THD)	≈ 1.3% (simulated)	≈ 2–4%	≈ 5–7%	≈ 5–8%	≈ 1–3%
Power Quality	High (near-sinusoidal output)	Good	Acceptable	Moderate	High
Modularity	Low	Low	Very Low	Very Low	High
Voltage Balancing	Not required	Not required	Required	Required	Not required
Scalability	Medium	Low	Low	Low	High
Hardware Cost	Low	Medium to High	Very High	Very High	High

Table 2. Comparative Analysis of 21-Level Inverter Topologies (with Actual Components).

The presented asymmetric 21-level inverter utilizes four DC sources of varying voltages to efficiently produce multiple stepped output levels. This is achieved with just eight power switches and four directional current control devices, significantly lowering the hardware requirements. In contrast to diode-clamped topologies, which may demand around 180 clamping diodes, and flying capacitor designs that require numerous capacitors and intricate voltage balancing methods, the proposed inverter maintains simplicity without sacrificing output quality. Simulations indicate a low total harmonic distortion (THD) near 1.3%, demonstrating a clean, sinusoidal voltage waveform. The elimination of voltage balancing mechanisms and minimized component usage make this design both cost-effective and compact, making it well-suited for renewable energy integration and medium-power applications.

VI. CONCLUSION

The proposed 21-level inverter successfully generates a well-regulated stepped final output voltage profile using a combination of multiple reference sine waves compared against a single high-frequency carrier signal. The design effectively utilizes only 8 active switches to synthesize 21 voltage levels, which significantly reduces the total harmonic content (THD) in the output and improves the waveform quality in contrast to traditional multilevel inverter designs. Simulation outcomes validate the effectiveness of the implemented switching strategy, where switches corresponding to lower voltage levels operate at higher frequencies, while those linked to higher levels switch less frequently, thereby optimizing switching losses. Additionally, the symmetrical voltage levels and balanced operation demonstrate that the modulation scheme is efficiently designed. This configuration is appropriate for applications in the medium-power range, especially in sustainable energy setups like photovoltaic-based grid connections, due to its reduced component count, enhanced output quality, and improved efficiency.

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